Notice of Allowability	Application No.	Applicant(s)	
	10/658,234	YANG ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *IDS (Apr 22, 2005), and Amdt/TD (Jul 1, 2005)*.

2. ☒ The allowed claim(s) is/are *1-8, 10-15, and 17-20 (now renumbered as 1-18, respectively for printing purposes)*.

3. ☒ The drawings filed on *08 September 2003* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 04222005
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's ~~Amendment~~/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

Response to IDS/Amendment/TD

The IDS submitted on Apr 22, 2005, and the amendment and terminal disclaimer submitted on Jul 1, 2005, were reviewed and considered with the following results:

The references on the IDS (which was received after the previous Office Action had been mailed) were both lined through since they had been already been considered, and they are cited on a previous PTO-892 (i.e. see paper no. 10272004).

The terminal disclaimer was approved and entered. This overcame the provisional double patenting of claims 1-8, and 10 with respect to co-pending application 10/637,146 (US 2005/0030105 A1). Therefore, the double patenting rejections have now been withdrawn.

Amended claim 15 overcame the objections to claims 15, and 17-20, which have also been withdrawn.

Amended claims 10 and 17 overcame their respective rejection under 35 U.S.C. 112 by changing their dependency from a previously cancelled claim to a proper, active claim. Therefore, these rejections have been withdrawn.

After reconsidering the claim language, and comments submitted by the applicants, as well as carefully considering related circuitry and their associated disclosures reviewed during several update type searches, the rejections of claims 1-7 under 35 U.S.C. 103(a), with respect to the separate Miyazawa and Yamamoto et al. references, have been withdrawn. There is no strong motivation to modify or combine either of these references, with each other or with any other reference(s), to ensure the bias control circuit (for a bias circuit with three transistors) has a

means for actively adjusting the equivalent resistance as recited within independent claim 1. Specific reasoning is described later under the Prior Art section.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance:

None of the prior art references reviewed and considered shows or discloses a bias control circuit, for a bias circuit comprising the first-third bias transistors having a specific configuration, as recited within independent claims 1, 8, and 15. More specifically, none of the references clearly shows or discloses a bias control circuit comprising: 1) means for actively adjusting the equivalent resistance between the first node and a reference voltage as recited within claim 1, upon which claims 2-7 depend; or 2) a bias control transistor and the (at least) first-fourth resistors connected to it as recited within claims 8 (upon which claims 10-14 depend) and 15 (upon which claims 17-20 depend). Since there is no strong motivation to modify or combine any prior art reference(s) to ensure those bias control circuit limitations are met (e.g. see the comments described later under the Prior Art section), the claims are deemed patentably distinct over the prior art of record.

Claims 1-8, 10-15, and 17-20 are allowed, and have been renumbered as claims 1-18, respectively for printing purposes. The renumbering takes into account the cancellation of claims 9 and 16.

Prior Art

The prior art references on the accompanying PTO-892 are cited for interest and documentation purposes only. Both of these references clearly show and disclose the bias circuit (with first-third bias transistors) and amplifier transistor as recited within each of the independent

claims. However, each reference shows only a single resistor coupled between the first node and ground (a known reference voltage). Miyazawa discloses that the value of resistor R1 can be changed to adjust current (e.g. see column 2, lines 17-26), but this resistor relates to one coupled between first bias transistor Q1 (e.g. see Fig. 13) and ground, not to resistor R3, which is coupled between the first node and ground. Fig. 4 of Kuriyama shows bias circuits I and II, wherein each bias circuit has its own respective first-third bias transistors coupled to a corresponding amplifier transistor (e.g. see Q4 and Q6). As with the other prior art references reviewed and considered, this reference does not clearly show or disclose the active adjustment of resistance R1 between the first node and ground as a means for adjusting operating characteristics of the overall bias circuit. Instead, the Kuriyama reference discloses that voltage Vref is determined in accordance with the base-emitter voltage of the transistor (e.g. see paragraph 0028), and by changing control signal Vcont, the amount of current can be switched (e.g. see paragraphs 0037 and 0038).

The following section refers back to references cited on previous PTO-892 forms submitted with earlier Office Actions (i.e. from 10272004 and 03232005) related to the present application. Although Fig. 5 of Miyazawa (i.e. reference US 6,566,954 cited in some of the previous Office Action's rejections) shows circuitry 31-34, which is different from a single resistor, coupled between the first node (e.g. base of third bias transistor 23) and ground, bias control voltage 31 provides the ability to control the amount of current flowing through the current mirror/source configuration (e.g. see column 7, lines 13-24), and therefore this bias control circuit does not actively adjust the resistance equivalence between the first node and ground. Finlay et al. discloses output current Ic relates to I_{REF} and R_{REF} (e.g. see column 2, line 55 to column 3, line 5), and it would be understood that these relate to the value of V_{REF}.

Although the reference shows different means (e.g. see Figs. 4-7) for controlling final amplifier transistor 32 (e.g. see Fig. 2), these means do not rely on actively adjusting the equivalent resistance of R_1 (shown in Fig. 2) that is coupled between first node 40 and ground. Shapiro et al. discloses that resistor 402 can be fixed or variable (e.g. see column 7, lines 5-7), voltage Vx is determined (at least in part) by the value of resistor 210 (e.g. see column 10, lines 3-4), and the relationship between voltage $V_{reference}$ (V_{ref}), resistor R (210), and current I_{ref} (e.g. shown in Fig. 2, disclosed on column 5, lines 24-40, and related to voltage V_{ref}, resistor 210, and current I_{ref} shown in Fig 11). However, resistor 210 relates to the resistance coupled between voltage V_{ref} and the bases of the first/second bias transistors T1/T3 (of Fig. 11). Therefore, the Shapiro reference does not clearly disclose any type of change with respect to the resistor/resistance (shown in Fig. 11) coupled between the base (i.e. the first node) of (third bias) transistor T2 and ground. Similar to Shapiro's circuit, Fowler discloses the relationship between voltage Vref, current Iref, and resistor 138 (e.g. see Fig. 1, and column 4, lines 1-12). This reference also shows/discloses means for making adjustments that do not affect the value of resistance between first node 140 and ground.

After reviewing and considering the applicants' comments, with respect to actively adjusting the equivalent resistance between the first node and a reference voltage (e.g. ground), and also carefully reconsidering the various prior art references reviewed, it was determined there is no strong motivation to replace a single, fixed resistor (e.g. a passive device that sets the bias voltage to the base of a transistor) with a means that will actively adjust the equivalent resistance at that position. For example, only one of the valid references (i.e. Miyazawa: US 6,566,954 does not have a common inventor, or assignee, with respect to the present application)

shows circuitry other than a single, fixed resistor coupled between the first node and ground, wherein that circuitry can be used to adjust the amount of current, not the resistance, as previously described above. Therefore, since there are already various known means for making adjustments to these types of bias circuits (i.e. having the specific first-third transistor configuration as cited), there is no strong motivation to add an additional adjusting means. For example, the bias circuit can already be adjusted by changing the value of: 1) the resistor coupled between the emitter of the first transistor/base of the amplifier transistor and ground; 2) the resistor coupled between a control signal (e.g. reference voltage) and the bases of the first/second bias transistors; or 3) the control signal/reference voltage coupled to the bases of the first/second bias transistors.

Any comments considered necessary by applicants must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE
Terry L. Englund

11 October 2005